

FIG. 1

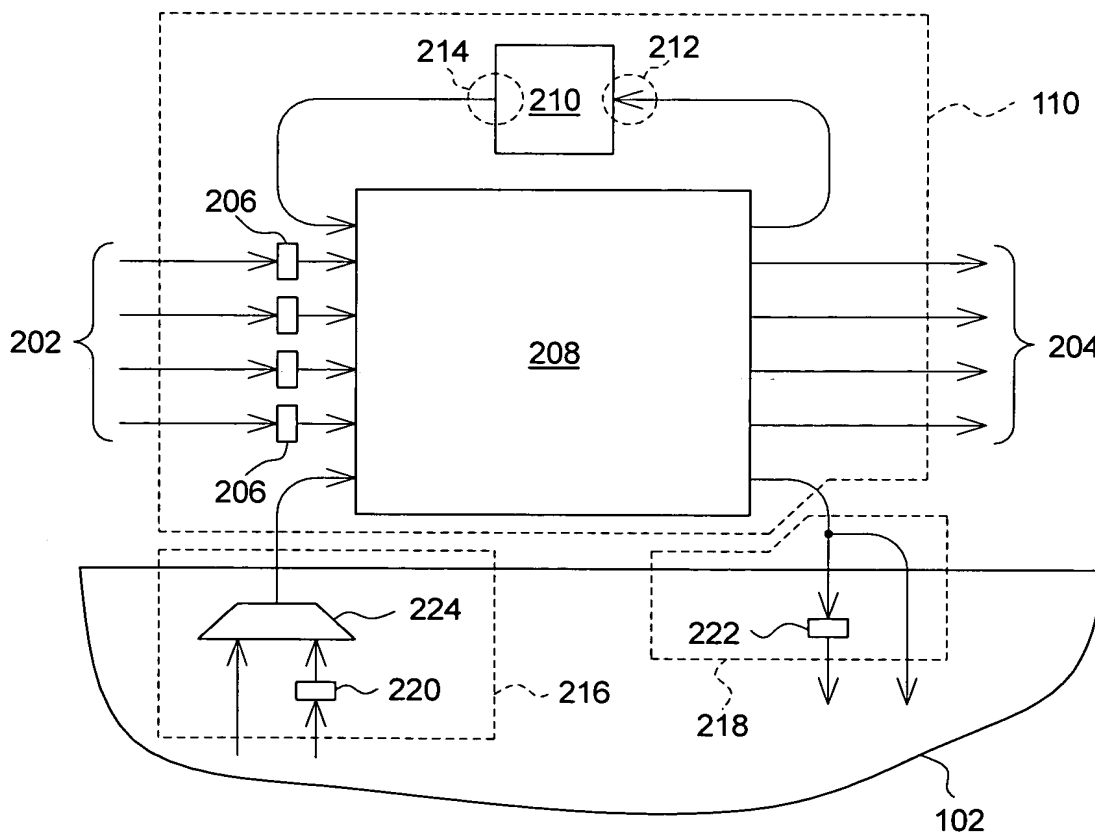


FIG. 2

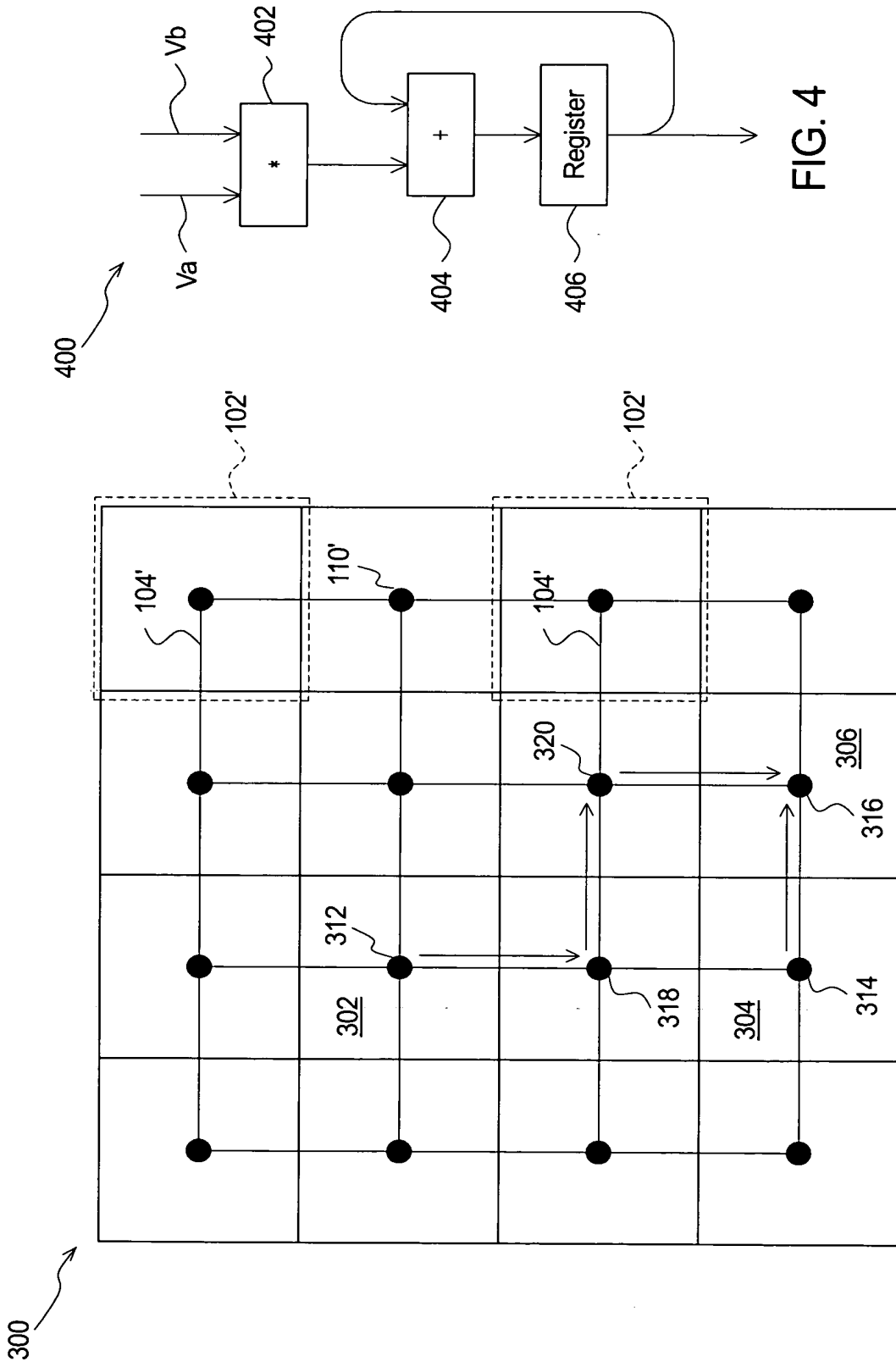


FIG. 4

FIG. 3

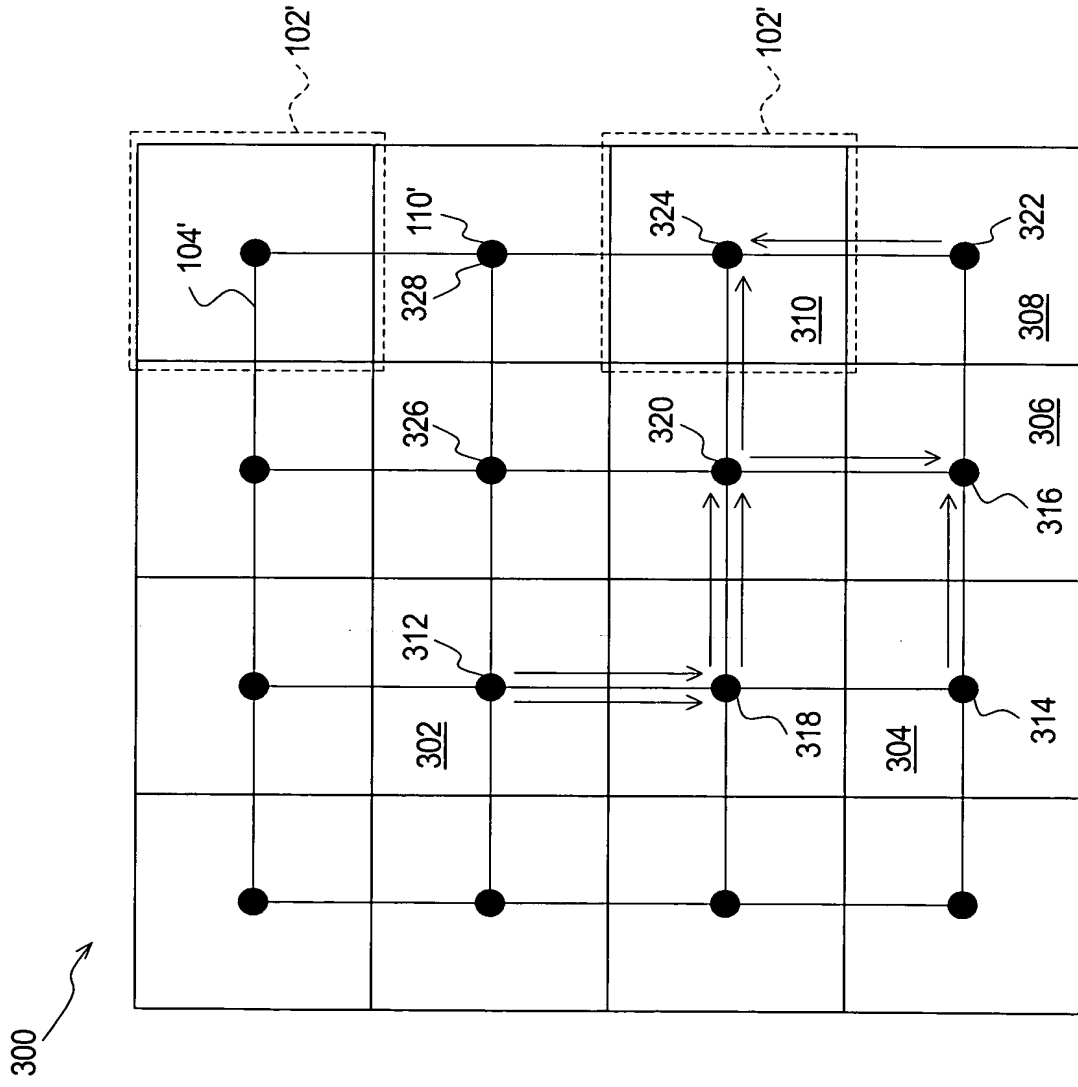


FIG. 5

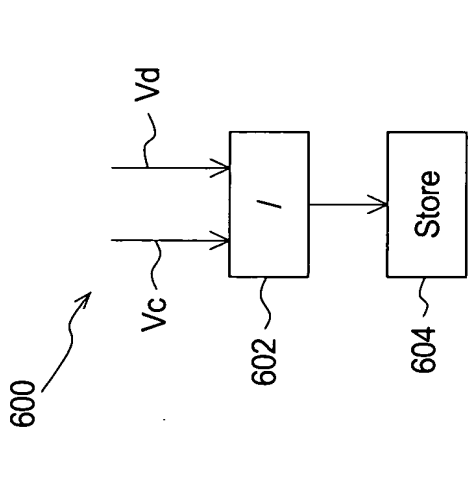


FIG. 6

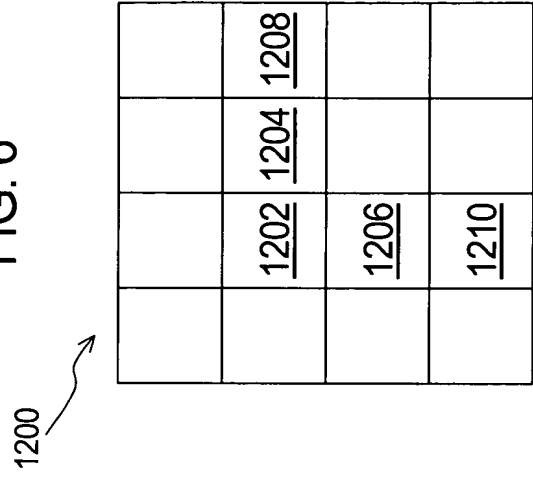


FIG. 12

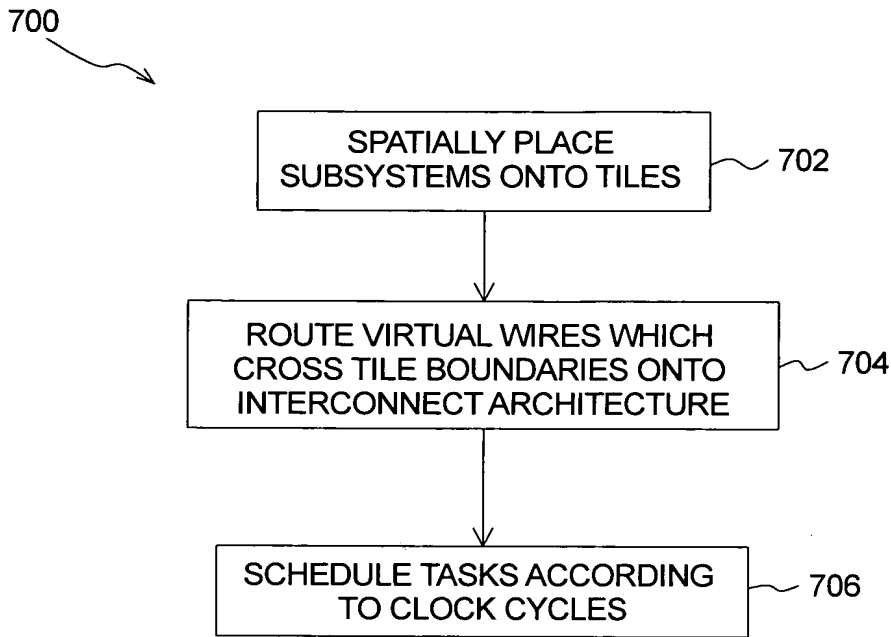


FIG. 7

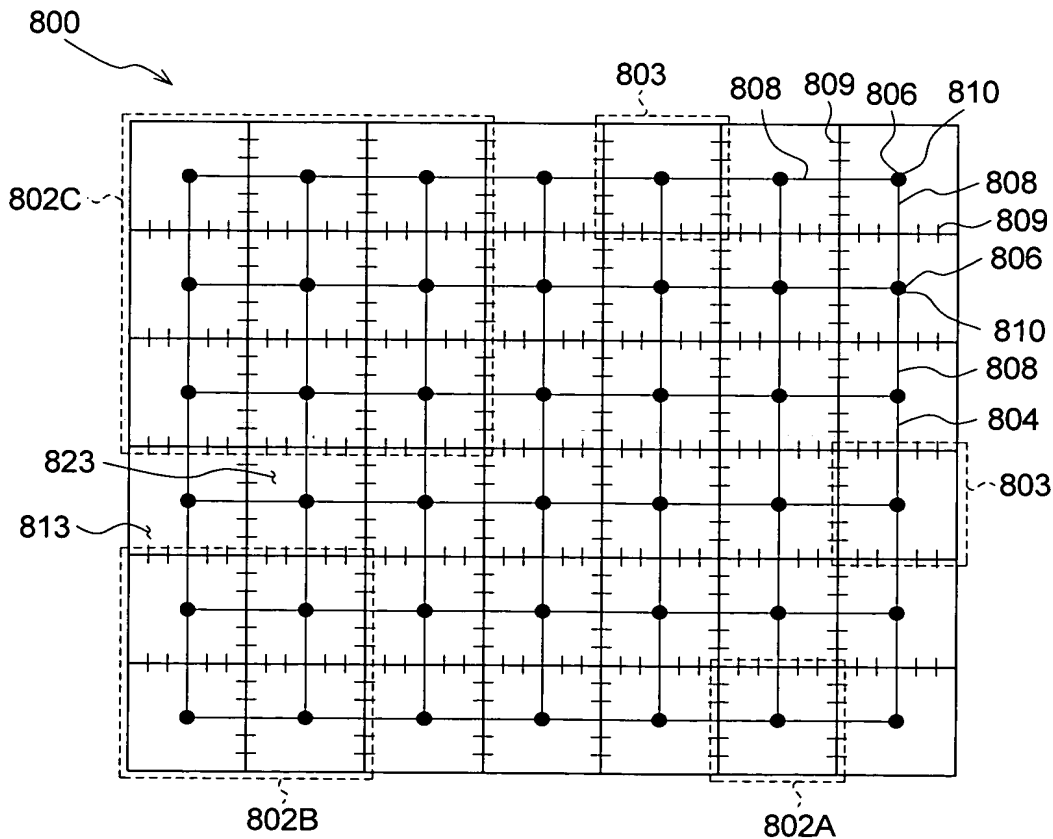


FIG. 8

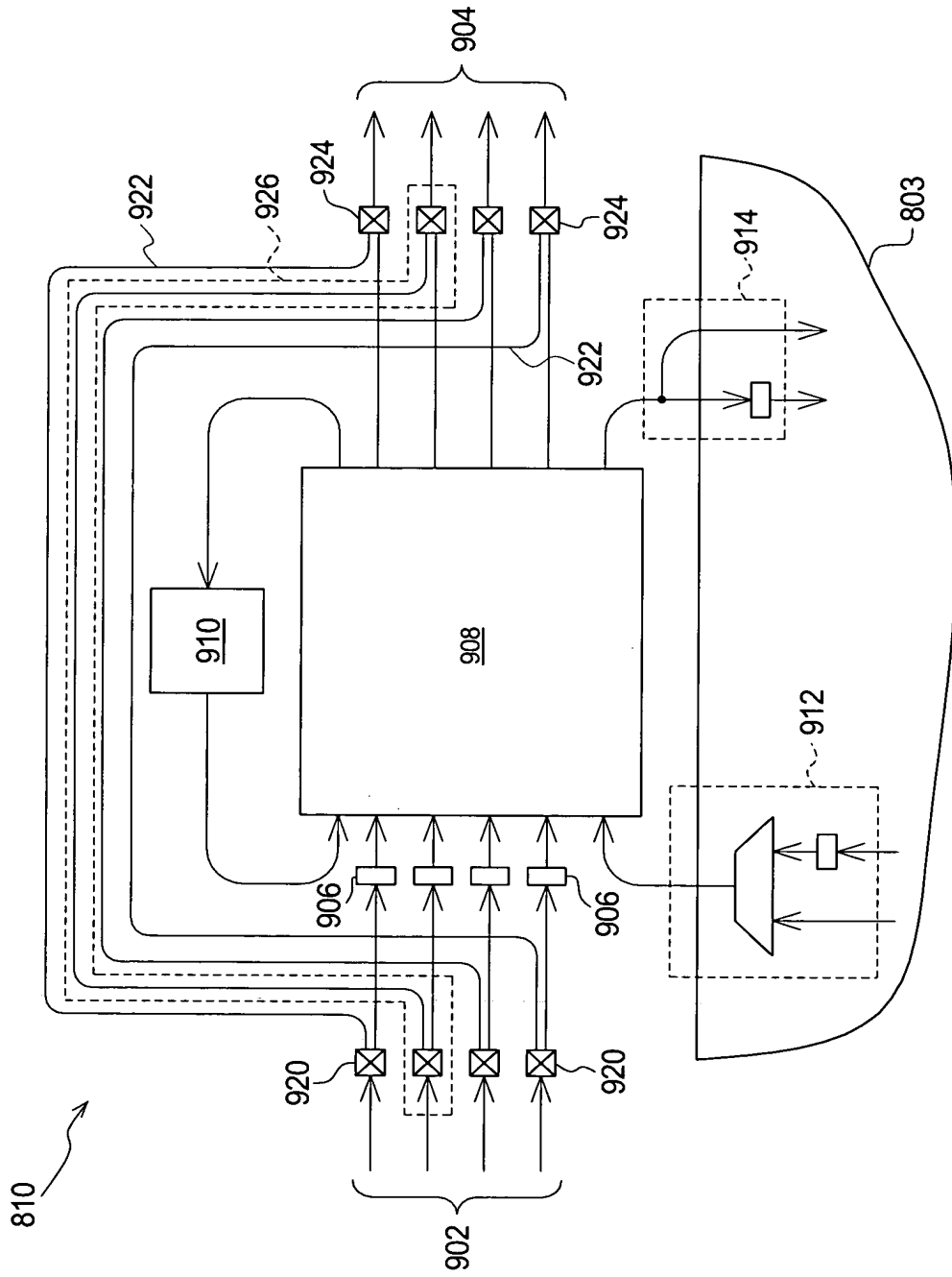


FIG. 9

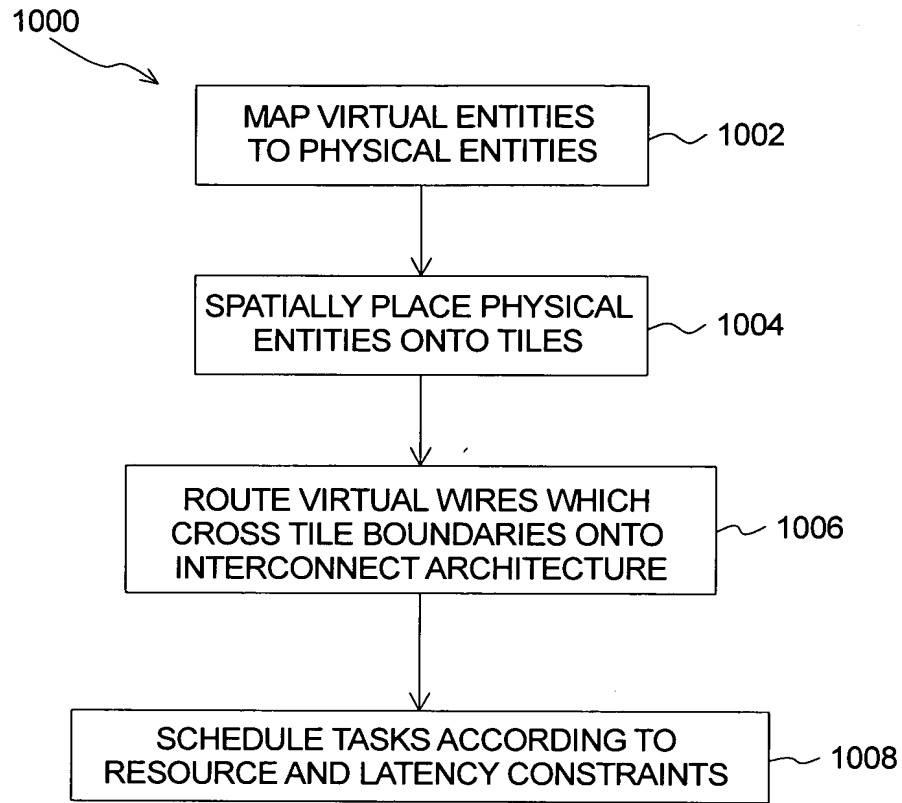


FIG. 10

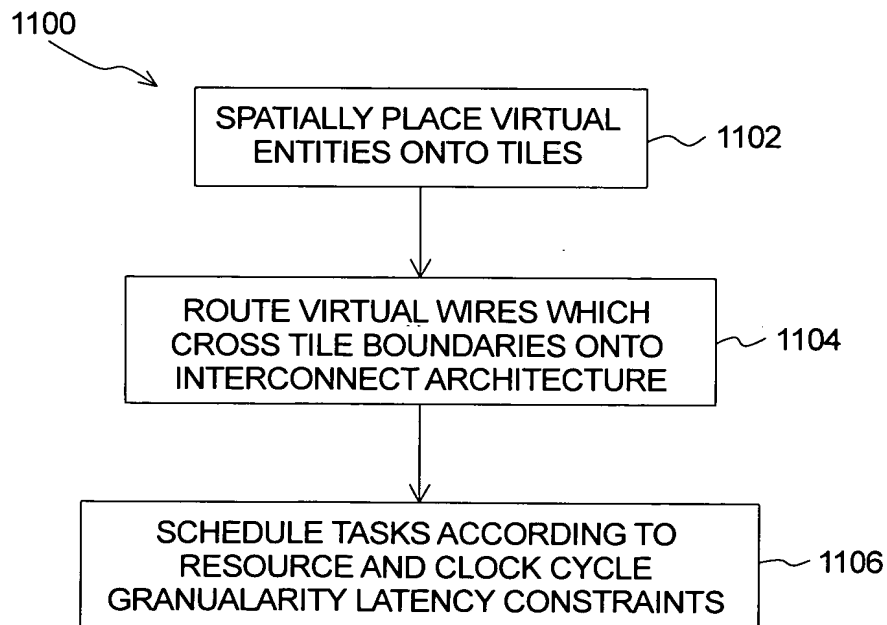


FIG. 11

Table 3					
Time	In tile 1206	Between tiles 1202 and 1206	In tile 1202	Between tiles 1202 and 1204	In tile 1204
1			$uAddr = a + 4$		
2			$wAddr = b + 8$	$uAddr$ transfers from 1202 to 1204	
3		$wAddr$ transfers from 1202 to 1206	$r = a + b$		$u = load(uAddr)$
4	$w = load(wAddr)$		$s = 5 + c$	$u$ transfers from 1204 to 1202	
5		$w$ transfers from 1206 to 1202	$x = u + r$		
6			$y = w + s$		
7			$z = s + r$		

FIG. 13

Table 4					
Time	In tile 1206	Between tiles 1202 and 1206	In tile 1202	Between tiles 1202 and 1208	In tile 1208
1			$uAddr = a + 4$		
2			$wAddr = b + 8$	$uAddr$ transfers from 1202 to 1204	
3		$wAddr$ transfers from 1202 to 1206	$r = a + b$	$uAddr$ transfers from 1204 to 1208	
4	$w = load(wAddr)$		$s = 5 + c$		$u = load(uAddr)$
5		$w$ transfers from 1206 to 1202	$z = s + r$	$u$ transfers from 1208 to 1204	
6			$y = w + s$	$u$ transfers from 1204 to 1202	
7			$x = u + r$		

FIG. 14

Table 5					
Time	In tile 1210	Between tiles 1202 and 1210	In tile 1202	Between tiles 1202 and 1204	In tile 1204
1			$wAddr = b + 8$		
2		wAddr transfers from 1202 to 1206	$uAddr = a + 4$		
3		wAddr transfers from 1206 to 1210	$r = a + b$	uAddr transfers from 1202 to 1204	
4	$w = \text{load}(wAddr)$		$s = 5 + c$		$u = \text{load}(uAddr)$
5		w transfers from 1210 to 1206	$z = s + r$	u transfers from 1204 to 1202	
6		w transfers from 1206 to 1202	$x = u + r$		
7			$y = w + s$		

FIG. 15